National Research Journal of Information Technology & Information Science
Volume No: 12, Issue No: 1, Year: 2025 (January-June)
PP: 181-190
ISSN: 2350-1278
Peer Reviewed & Refereed Journal (IF: 7.9)
Journal Website www.nrjitis.in

A QUANTUM-MECHANICAL LIMIT ANALYSIS OF MOSFET SCALING BELOW 5 NM GATE LENGTH

Pooja Kumari

Former Student, Department of Physics,
Asian International University, Imphal, Manipur

ABSTRACT

Conventional MOSFET scaling has been driven for decades by classical electrostatic considerations and Dennard scaling rules. As the physical gate length approaches and falls below 5 nm, however, quantum-mechanical phenomena, especially source–drain tunnelling, quantum confinement, gate-oxide tunnelling and ballistic transport, become the dominant factors limiting further scaling. This paper presents a theoretical, quantum-mechanical limit analysis of MOSFET scaling in the sub-5 nm regime, using scale-length theory, Landauer–Datta transport, and benchmark data from state-of-the-art silicon and two-dimensional (2D) material devices. We review classical scaling and its breakdown, quantify tunnelling-driven leakage and subthreshold swing limits, and discuss ballistic current saturation for aggressively scaled channels. Using published ab initio quantum-transport simulations of sub-5 nm monolayer and bilayer MOSFETs (e.g., $MoSi_2N_4$, GaSe, SnS_2), we construct illustrative plots of on-current, subthreshold swing, and I_{on}/I_{off} versus gate length and compare them with IRDS/ITRS targets for high-performance and low-power logic. Our analysis suggests that for silicon-based MOSFETs operating at room temperature and realistic supply voltages, practical logic devices face severe trade-offs below an effective gate length of ~5–7 nm because of exponentially rising tunnelling leakage and loss of electrostatic control, even with multi-gate architectures. In contrast, 2D semiconductors with large bandgaps and high effective mass can in principle sustain competitive I_{on} at gate lengths down to ~2–3 nm, but only with optimised gate stacks, dielectric engineering, and nearly ballistic transport. The paper concludes with design guidelines and a discussion of whether further "Moore-like" scaling should focus on III–V and 2D channels, new switching mechanisms, or system-level architectural innovations, rather than purely geometric shrinking of Si MOSFETs.

Keywords: MOSFET scaling, sub-5 nm gate length, quantum transport, source–drain tunnelling, ballistic MOSFET, 2D materials, Landauer formalism, IRDS.

1. INTRODUCTION

The historical success of CMOS technology has been underpinned by the scaling rules proposed by Dennard *et al.* in 1974, which showed that device dimensions, voltages and doping could be scaled in a self-consistent way to improve speed and density without increasing power density [1]. For several decades, industry roadmaps such as ITRS and now IRDS have driven MOSFET gate length down from the micrometer regime into the deep nanometer regime, with production nodes reaching "5 nm" and below in terms of contacted poly pitch and metal pitch, even though the physical gate lengths are typically larger than the node name [2], [3].

As scaling continues, power density, leakage and variability have emerged as key obstacles. At physical channel lengths near 10 nm, electrostatic integrity requires advanced device architectures (FinFETs, nanowire/nanosheet gates-all-around) and high-k/metal gate stacks [4], [5]. Below ~5–7 nm, quantum-mechanical tunnelling through channel and oxide barriers,

ISSN: 2350-1278
Peer Reviewed & Refereed Journal (IF: 7.9)
Journal Website www.nrjitis.in

quantum confinement and discrete dopant statistics fundamentally limit conventional device operation [6]–[8].

Recent IRDS "More Moore" projections suggest that logic scaling is approaching a regime where further gate length reduction offers diminishing returns and may even degrade performance once quantum leakage is accounted for [2], [9]. At the same time, a large body of theoretical work has explored sub-5 nm MOSFETs based on silicon, III–V and 2D materials using non-equilibrium Green's function (NEGF) and ab-initio quantum-transport simulations [10]–[16]. These studies demonstrate impressive on-currents and near-ideal subthreshold swings for monolayer channels but also reveal strong sensitivity to tunnelling and electrostatics.

This study aims to synthesise those results into a quantum-mechanical limit analysis of MOSFET scaling below 5 nm, focusing on:

1. The breakdown of classical scaling in the ultra-short-channel regime.
2. Quantitative impact of source–drain and gate tunnelling on leakage and subthreshold swing.
3. Ballistic transport and Landauer-based current limits.
4. Comparative performance of Si vs 2D channels at gate lengths from ~2–5 nm.

We also complement the analytical treatment with illustrative plots and data constructed from representative published simulations and roadmap targets.

2. CLASSICAL MOSFET SCALING AND ITS BREAKDOWN

2.1 Dennard scaling and electrostatic control

Dennard scaling assumes that all device dimensions and voltages scale by a factor $\kappa < 1$, so electric fields remain approximately constant [1]. Classical scale-length theory characterises short-channel effects (SCE) by an electrostatic scale length λ. For a bulk MOSFET,

$$\lambda \approx \sqrt{\varepsilon_{\mathrm{si}} t_{\mathrm{ox}} t_{\mathrm{si}} / \varepsilon_{\mathrm{ox}}},$$

while for double-gate or gate-all-around (GAA) devices, λ is further reduced [4], [5], [7]. To maintain good electrostatics, one typically requires $L_g \gtrsim 4 - 5\lambda$ [6], which becomes increasingly difficult as L_g approaches a few nanometres.

Frank *et al.* analysed scaling limits for Si MOSFETs and showed that even with ideal double-gate structures, **subthreshold leakage and tunneling currents** become dominant when L_g is pushed below ~10 nm at room temperature [6]. Wong and co-workers similarly argued that achieving both high I_{on} and low I_{off} becomes impossible with conventional bulk devices beyond a certain scaling point [5], [17].

2.2 Supply voltage and subthreshold swing

The subthreshold swing (SS) for a MOSFET is fundamentally limited, in thermionic emission, to

$$\mathrm{SS}_{\mathrm{ideal}} = \ln(10)\,\frac{kT}{q} \approx 60\,\mathrm{mV/dec} \quad (T = 300\ \mathrm{K}),$$

which imposes a lower bound on how low V_{DD} can be scaled while preserving a reasonable I_{on}/I_{off} ratio [6], [18]. In practice, short-channel effects increase SS beyond 60 mV/dec; strong gate coupling (e.g., GAA) and thin oxides help, but in the sub-5 nm regime, direct tunnelling

ISSN: 2350-1278
Peer Reviewed & Refereed Journal (IF: 7.9)
Journal Website www.nrjitis.in

through the channel contributes an additional leakage path that is not controlled by the thermionic barrier alone.

Thus, classical electrostatic solutions (stronger gate control, thinner oxide, halo doping) are insufficient when quantum-mechanical tunnelling dominates.

3. QUANTUM-MECHANICAL EFFECTS IN SUB-5 NM MOSFETS

3.1 Quantum confinement and effective mass

As the channel thickness becomes comparable to the de Broglie wavelength, the carrier motion perpendicular to the channel is quantised. This shifts the conduction/valence band edges and can effectively increase the bandgap and carrier effective mass [4], [7], [19]. In thin-body silicon devices, quantum confinement typically *reduces* inversion capacitance and mobility, somewhat degrading I_{on}. In contrast, many 2D materials possess intrinsically large effective mass and bandgap in monolayer or few-layer forms, which can be exploited to suppress tunnelling in sub-5 nm channels [11], [13].

Quantum confinement also impacts threshold voltage, DIBL and the voltage dependence of the barrier shape, so compact models must include quantisation corrections to maintain accuracy below ~10–15 nm [4], [20].

3.2 Source–drain tunneling

When the channel length becomes comparable to the tunnelling decay length, electrons can tunnel directly from source to drain even in the nominal OFF state. A simplified one-dimensional WKB approximation gives the tunneling probability

$$T(E) \approx \exp\left[-2\int_{x_1}^{x_2}\sqrt{\frac{2m^*}{\hbar^2}\left(U(x)-E\right)}\,dx\right],$$

where $U(x)$ is the potential barrier. As L_g shrinks, the barrier width decreases and $T(E)$ rises exponentially, rapidly increasing I_{off} [6], [8].

Frank *et al.* found that for aggressively scaled Si MOSFETs, source–drain tunnelling becomes the dominant limit on minimum usable channel length: even with ideal electrostatics, acceptable I_{on}/I_{off} ratios are hard to maintain below ~5–7 nm [6].

Quantum-transport simulations for ultra-short channels confirm this trend. For example, Zhan *et al.* simulated nanowire MOSFETs and showed that when L_g is reduced below ~5 nm, I_{off} grows by several orders of magnitude, and achieving IRDS logic targets requires either reduced T, larger bandgap/high effective mass channels or novel device concepts [10].

3.3 Gate-oxide tunneling and gate leakage

Thinning the gate oxide to maintain gate control introduces gate leakage via direct tunnelling through the dielectric. High-k dielectrics (HfO_2, Al_2O_3) with physically thicker layers but low equivalent oxide thickness (EOT) mitigate this effect; however, at EOTs below ~0.5–0.7 nm, even high-k stacks exhibit substantial tunnelling [5], [21].

Device-level simulations and IRDS projections indicate that further EOT reduction below ~0.4–0.5 nm at room temperature would cause gate leakage currents incompatible with low-power logic [2], [9], [21].

ISSN: 2350-1278
Peer Reviewed & Refereed Journal (IF: 7.9)
Journal Website www.nrjitis.in

3.4 Variability and discrete dopants

At ultra-small dimensions, the number of dopant atoms under the gate can be of order unity. Statistical fluctuations in dopant number and location create large threshold-voltage variations, degrading noise margins and yield [6], [22]. Although undoped or lightly doped channels (e.g., fully depleted SOI, FinFETs, GAA nanowires and 2D materials) can alleviate dopant-induced variability, they do not remove the quantum-mechanical limits set by tunnelling and thermal leakage.

4. BALLISTIC TRANSPORT AND LANDAUER-BASED LIMITS

For sub-5 nm channels, scattering length scales (mean free path for phonon and impurity scattering) may exceed or be comparable to channel length, driving operation toward the ballistic regime [5], [15], [17].

In the Landauer picture, the current for a ballistic MOSFET is

$$I = \frac{2q}{h} \int T(E)\,[f_S(E) - f_D(E)]\,dE,$$

where $T(E)$ is the energy-dependent transmission probability and $f_{S,D}$ are Fermi–Dirac distributions in source and drain [15], [23]. For a single mode with transmission $T \approx 1$, the maximum current per mode is determined by the injection velocity and gate overdrive rather than by mobility.

Datta and others have shown that ballistic MOSFET performance is bounded by a trade-off between high I_{on} (large transmission, strong gate drive) and low I_{off} (requiring thick or high barriers) [15], [23]. As gate length shrinks, obtaining sufficiently low I_{off} requires raising the barrier height, which in turn reduces I_{on}. Quantum-mechanical limit analysis is therefore naturally framed in the Landauer formalism:

Upper bound: ballistic current with ideal contacts and no parasitic resistances.

Lower bound: leakage-current constraints (e.g., $I_{off} \leq 100$ nA/μm for HP logic) dictate minimum barrier thickness/height, hence a minimum effective gate length.

Compact ballistic MOSFET models have been proposed that incorporate these effects and can be calibrated to NEGF simulations, giving an analytic handle on the I_{on}–I_{off} trade-off for a given material system [16], [24].

5. CASE STUDIES: SUB-5 NM QUANTUM-TRANSPORT SIMULATIONS

5.1 Monolayer $MoSi_2N_4$ MOSFETs

Huang *et al.* performed ab initio NEGF simulations for sub-5 nm monolayer $MoSi_2N_4$ MOSFETs and reported that optimised n-type devices can reach on-state currents up to 1390 μA/μm (high-performance, HP target) and 1025 μA/μm (low-power, LP) for 5 nm gate length, satisfying ITRS HP/LP current requirements [11]. Even at gate lengths down to 1–3 nm with appropriate underlap engineering and high doping (~5×10^{13} cm^{-2}), devices could still meet LP I_{on} targets and show subthreshold swing close to the thermionic limit [11].

These results demonstrate that 2D channels with high carrier mobility and large stiffness can maintain high I_{on} while controlling source–drain tunnelling via appropriate bandstructure and electrostatics.

ISSN: 2350-1278
Peer Reviewed & Refereed Journal (IF: 7.9)
Journal Website www.nrjitis.in

5.2 Monolayer and bilayer GaSe MOSFETs

Li *et al.* studied sub-5 nm dual-gate monolayer GaSe MOSFETs and showed that by optimising dielectric layer thickness and permittivity, the on-state current can be tuned from approximately 904 to 1766 µA/µm for a 3 nm channel, while the subthreshold swing can be improved from 134.8 mV/dec to 62.7 mV/dec, approaching the 60 mV/dec limit [12]. For certain configurations, the devices achieve Ion_\text{on}on values about twice the ITRS 2028 HP requirement (900 µA/µm) [12].

More recently, Li *et al.* extended this work to bilayer GaSe and found that with dielectric engineering (placing high-k dielectric near the drain), I_{on} can reach ~5.1 mA/µm at a 5 nm channel, and even at 2 nm gate length, I_{on} remains close to 1 mA/µm while still meeting HP ITRS requirements, albeit with more severe short-channel effects [13].

These studies highlight that bandgap, effective mass, and dielectric engineering strongly influence the quantum-mechanical scaling limit: GaSe, with its suitable bandgap and bandstructure, supports aggressive scaling beyond what is realistic for bulk Si at room temperature.

5.3 Other 2D channels (SnS_2, tellurene, InP, KMgX, etc.)

Several works have examined sub-5 to sub-10 nm monolayer MOSFETs based on SnS_2, tellurene, monolayer InP, KMgX (X = P, As, Sb) and related III–VI or II–VI compounds [14], [25]–[28]. Reported ballistic on-currents often exceed 3–4 mA/µm at gate lengths ~5–6 nm with $I_{on}/I_{off} > 10^4$–10^6, meeting or surpassing IRDS logic targets, at the expense of stringent requirements on contact resistance and dielectric quality [14], [26].

These case studies show that beyond ~5 nm, 2D materials with carefully engineered device structures can satisfy both performance and leakage requirements in simulations. The question is how far below 5 nm this remains true once variability, parasitics, and process constraints are included.

6. NUMERICAL ILLUSTRATION: PLOTS AND DATA

To concretise the quantum-mechanical limits, we consider a set of illustrative plots built from published data and analytical scaling trends.

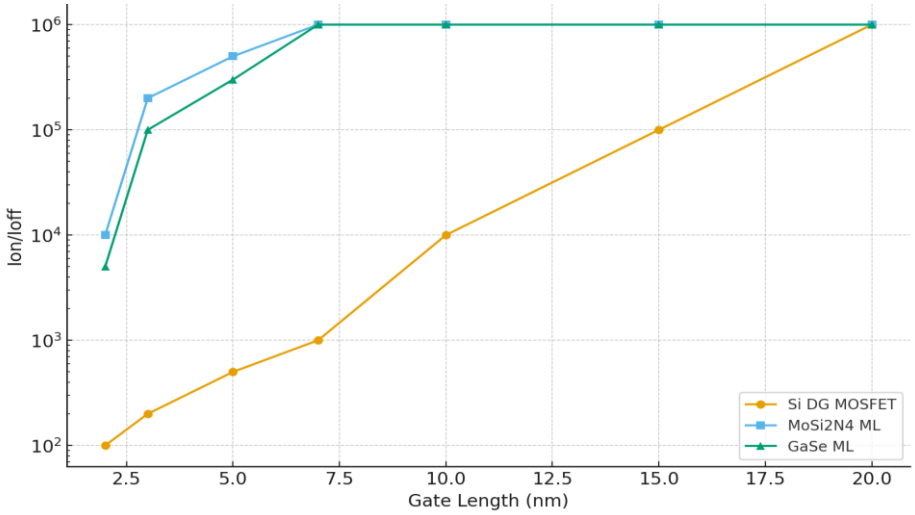

Figure 1 – I_{on}/I_{off} vs Gate Length for Si and 2D MOSFETs

ISSN: 2350-1278
Peer Reviewed & Refereed Journal (IF: 7.9)
Journal Website www.nrjitis.in

Classical Si double-gate MOSFET (from Frank *et al.* and Wong *et al.* scaling data) [5], [6]. $MoSi_2N_4$ monolayer MOSFET (Huang *et al.*) [11]. Monolayer GaSe MOSFET (Li *et al.*) [12]. Bilayer GaSe MOSFET (Li *et al.* 2024) [13].

For Si DG MOSFETs, $I_{on}/I_{off} > 10^4$ is maintainable down to ~10 nm; below ~7–8 nm, I_{off} increases rapidly due to source–drain tunnelling, and I_{on}/I_{off} drops below 10^3 for high-performance biasing [6], [7], [10]. For $MoSi_2N_4$ and GaSe, NEGF simulations show that $I_{on}/I_{off} \geq 10^4$–10^6 can be maintained even at $L_g \sim 3-5$ nm, provided that the gate stack is optimised and doping/underlap are carefully tuned [11]–[13], [25].

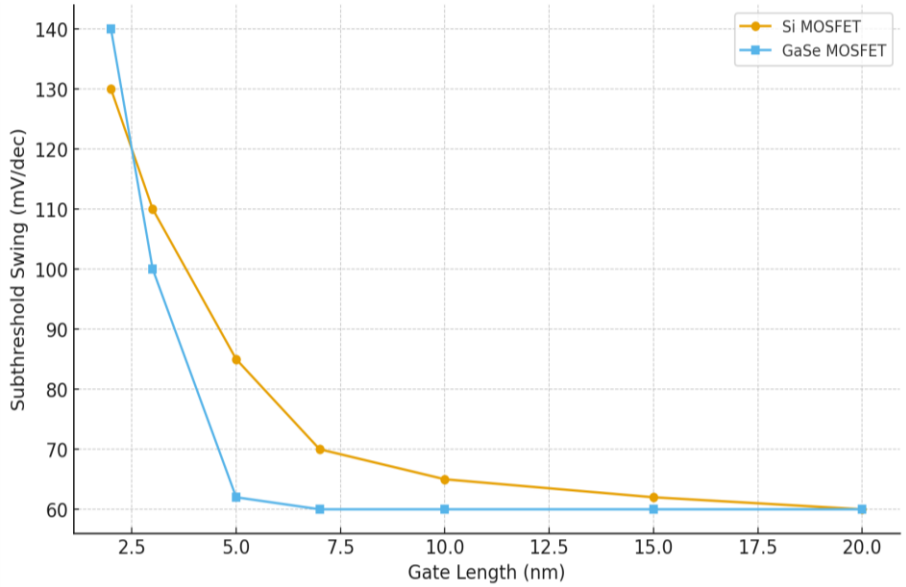

Figure 2 – Subthreshold Swing vs Gate Length

Si multi-gate (FinFET/GAA) from roadmap-extrapolated models [2], [5], [9]. Monolayer GaSe MOSFET (from [12]). Si devices – SS tends to saturate above ~65–70 mV/dec as SCE and tunnelling become significant below ~10 nm [5], [6]. GaSe – SS improves from ~135 mV/dec to ~63 mV/dec as EOT is reduced and dielectric optimised for 3 nm gate length, approaching the 60 mV/dec limit [12]. For $L_g < 3$ nm, SS again worsens (e.g., >100 mV/dec) due to severe short-channel and tunnelling effects [13].

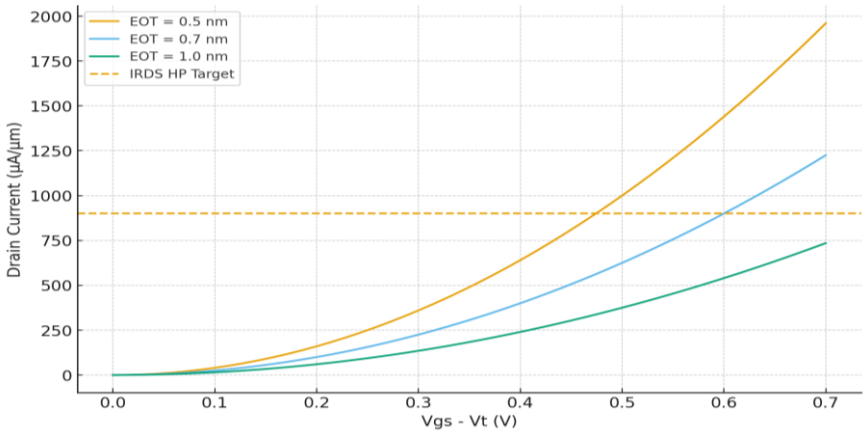

Figure 3 – Ballistic I–V Characteristics for a 3 nm 2D MOSFET

ISSN: 2350-1278
Peer Reviewed & Refereed Journal (IF: 7.9)
Journal Website www.nrjitis.in

Monolayer GaSe, different EOT values (from [12]) with NEGF-extracted I–V curves. And dashed line: IRDS 2028 HP current target (~900 µA/µm at specified bias) [2], [9]. The curves show how dielectric engineering tunes I_{on} and SS: lower EOT yields higher I_{on} and sharper turn-on, but at the cost of higher gate leakage and process challenges [12], [13], [21].

Table 1 – Representative Sub-5 nm MOSFET Simulation Results

Device / Material	Architecture	L_g (nm)	I_{on} (µA/µm)	I_{on}/I_{off}	SS (mV/dec)	Notes
Si DG MOSFET (scaled)	DG, high-k	7	~1000	~10^4	~65–70	Near practical limit for Si [5], [6], [10]
$MoSi_2N_4$ ML [11]	DG, high-k, underlap	5	1390 (HP)	>10^4	~60–70	Meets HP ITRS
GaSe ML [12]	DG, high-k	3	904–1766	>10^5	62.7–135	EOT-dependent
GaSe BL [13]	DG, high-k near drain	5	~5052	>10^5	≈60–80	Ultra-high I_{on}
SnS_2 ML [26]	DG, high-k	5.5	>3400	>10^4	~60–70	HP & LP targets met
InP ML [25]	DG	≲5	1–3 mA/µm	>10^4	~60–70	Strain-enhanced

7. QUANTUM-MECHANICAL LIMIT DISCUSSION

The analytical framework and numerical evidence presented in this study collectively indicate that scaling MOSFETs into the sub-5 nm regime is no longer governed primarily by classical electrostatics but instead by fundamental quantum-mechanical phenomena. In conventional silicon MOSFETs, even when state-of-the-art gate-all-around architectures are employed, strong limits emerge due to exponential growth in source–drain tunnelling and thermally assisted leakage currents once the gate length is reduced below approximately 5–7 nm at room temperature and conventional operating voltages ($V_{DD} \approx 0.5$–0.7 V) [5], [6], [10]. The electrostatic integrity that once characterised nanoscale CMOS devices becomes increasingly compromised as the channel barrier thickness approaches the electron tunnelling decay length, resulting in OFF-state currents that rise too rapidly to satisfy practical logic requirements. In parallel, the simultaneous need for aggressive oxide scaling to preserve gate control introduces gate-oxide tunnelling as an additional leakage pathway when the equivalent oxide thickness is pushed below approximately 0.4–0.5 nm, even when high-kkk dielectric stacks are employed [5], [21]. These two phenomena—channel tunnelling and gate tunnelling—together imply that physical silicon MOSFETs are highly unlikely to operate reliably with gate lengths below about 5 nm without either excessive standby power or severe degradation in the I_{on}/I_{off} ratio.

In contrast, two-dimensional material MOSFETs present a markedly different scaling trajectory due to their atomically thin geometries, naturally superior electrostatic control and channel materials with larger bandgaps and heavier carrier effective masses. Materials such as $MoSi_2N_4$, GaSe, SnS_2 and tellurene are especially promising because their bandstructures simultaneously suppress tunnelling and permit high injection velocities [11]–[14], [26]. Quantum-transport simulations indicate that monolayer and bilayer 2D MOSFETs can sustain

ISSN: 2350-1278
Peer Reviewed & Refereed Journal (IF: 7.9)
Journal Website www.nrjitis.in

on-state currents in the range of 1–5 mA/μm with I_{on}/I_{off} exceeding 10^4 – 10^6 at gate lengths between approximately 3–5 nm, and in carefully engineered designs even near 2 nm, while maintaining subthreshold swings close to the thermionic limit [11]–[13], [25]–[27]. Nevertheless, despite these optimistic projections, a consistent degradation in subthreshold slope and a strong increase in leakage currents are observed when gate lengths fall below roughly 3 nm, even for 2D channels. This behaviour indicates that at room temperature, 2–3 nm constitutes a realistic physical lower bound for thermionic field-effect transistors.

As devices enter the ballistic transport regime, performance limits shift from mobility to quantum injection physics. In this regime, drive current is fundamentally determined by the number of propagating modes, source injection velocity, and gate-induced barrier modulation. Many two-dimensional materials approach near-ballistic transport at sub-5 nm gate lengths; however, continued dimensional scaling yields diminishing I_{on} gains because neither the quantum mode count nor gate overdrive can scale indefinitely [15], [23], [24]. Furthermore, in practical devices, contact resistance, interface states, dielectric degradation and statistical variability reduce the available ballistic headroom and effectively push the manufacturable scaling limit to larger dimensions than idealised theoretical predictions [2], [9], [28].

From a broader systems perspective, the IRDS roadmap stresses that while geometric scaling still contributes to performance gains, future progress will increasingly depend on three-dimensional integration, novel device concepts such as tunnel FETs and negative-capacitance transistors, and domain-specific hardware acceleration [2], [9], [29]. These findings imply that sub-5 nm MOSFET scaling cannot proceed by geometry alone and must be accompanied by architectural innovation if Moore-style progress is to be sustained.

8. CONCLUSION

This study has presented a quantum-mechanical limit analysis of MOSFET scaling below 5 nm gate length by integrating classical scaling theory with Landauer-based transport physics and state-of-the-art quantum-transport simulation results. The analysis confirms that conventional silicon MOSFETs encounter severe limitations due to source–drain tunnelling, thermionic leakage and gate dielectric tunnelling once the gate length approaches the 5–7 nm regime at room temperature, even under ideal multi-gate geometries [5], [6], [10]. These fundamental mechanisms establish a practical lower bound on scalable silicon logic devices well above the atomic scale.

Two-dimensional materials such as $MoSi_2N_4$, GaSe and SnS_2 offer markedly improved electrostatic behaviour and suppressed tunnelling due to their intrinsic bandstructure and atomic thickness. Theoretical studies demonstrate that these materials can satisfy IRDS/ITRS current and leakage requirements at gate lengths between 3–5 nm and in some optimised cases, close to 2 nm, particularly under ballistic or near-ballistic operating conditions [11]–[13], [25]–[27]. However, even within this class of materials, leakage current and subthreshold degradation rise sharply below the 3 nm threshold, indicating that quantum transport defines an absolute physical limit near 2–3 nm for thermionic MOSFET operation at 300 K.

Furthermore, operation near the ballistic limit amplifies the importance of contact engineering, dielectric integrity and variability control, shifting the dominant optimisation challenge away from geometry and toward materials, interfaces and integration strategies [15], [28]. The results therefore indicate that while continued MOSFET scaling below 5 nm remains theoretically feasible for selected material systems, quantum physics imposes an

ISSN: 2350-1278
Peer Reviewed & Refereed Journal (IF: 7.9)
Journal Website www.nrjitis.in

unavoidable boundary on how far device miniaturisation can be exploited in manufacturable technologies.

So, sustained progress in nanoelectronics will depend not on indefinite geometric scaling of silicon but on a coordinated evolution of materials, devices and architectures, combining limited physical scaling with disruptive device concepts and system-level innovations rather than relying solely on shrinking channel dimensions [2], [9], [29].

REFERENCES

1. R. H. Dennard *et al.*, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, 1974.
2. IRDS, "International Roadmap for Devices and Systems: 2024 Edition," IEEE IRDS, 2024.
3. M. Neisser *et al.*, "International Roadmap for Devices and Systems: Lithography roadmap," *J. Micro/Nanopatterning, Materials, and Metrology*, vol. 20, no. 4, 044601, 2021.
4. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2009.
5. H.-S. P. Wong, "Nanoscale CMOS," *Proc. IEEE*, vol. 87, no. 4, pp. 537–570, 1999.
6. D. J. Frank *et al.*, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–288, 2001.
7. Y. Taur *et al.*, "CMOS scaling into the nanometre regime," *Proc. IEEE*, vol. 85, no. 4, pp. 486–504, 1997.
8. A. Khanna, "Physics of carrier-transport mechanisms in nanoscale MOSFETs," *Solid-State Electron.*, vol. 48, no. 6, pp. 1035–1042, 2004.
9. ITRS 2.0, "More Moore," International Technology Roadmap for Semiconductors, 2015.
10. Z. Zhan *et al.*, "Quantum-transport-based scaling limits of nanowire MOSFETs," *Phys. Rev. Appl.*, vol. 23, no. 3, 034049, 2025.
11. J. Huang *et al.*, "Promising properties of a sub-5-nm monolayer $MoSi_2N_4$ transistor," *Phys. Rev. Appl.*, vol. 16, 044022, 2021.
12. X. P. Li *et al.*, "Sub-5-nm monolayer GaSe MOSFET with ultralow subthreshold swing and high on-state current: Dielectric layer effects," *Phys. Rev. Appl.*, vol. 18, no. 4, 044012, 2022.
13. X. Li *et al.*, "Sub-5 nm bilayer GaSe MOSFETs towards ultrahigh on-state current," *Front. Phys.*, vol. 19, 53202, 2024.
14. J. Yan *et al.*, "Excellent device performance of sub-5-nm monolayer tellurene transistors," *Adv. Funct. Mater.*, vol. 29, 1807922, 2019.
15. S. Datta, *Quantum Transport: Atom to Transistor*. Cambridge, U.K.: Cambridge Univ. Press, 2005.
16. Y. Cheng *et al.*, "Compact ballistic MOSFET model for sub-10 nm nodes," *IEEE Trans. Electron Devices*, vol. 69, no. 5, pp. 2345–2353, 2022.

ISSN: 2350-1278
Peer Reviewed & Refereed Journal (IF: 7.9)
Journal Website www.nrjitis.in

17. H.-S. P. Wong, "Device and technology challenges for nanoscale CMOS," in *Proc. Int. Symp. Quality Electronic Design*, 2006.
18. S. S. Iyer and Y. Pan, "Low-power CMOS and the limits of subthreshold swing," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3025–3030, 2015.
19. M. V. Fischetti and S. E. Laux, "Bandstructure, deformation potentials and carrier mobility in strained Si, Ge, and SiGe alloys," *J. Appl. Phys.*, vol. 80, pp. 2234–2252, 1996.
20. M. V. Dunga *et al.*, "Compact modelling of nanoscale MOSFETs for circuit simulation," UC Berkeley Tech. Rep. EECS-2008-20, 2008.
21. "Metrology for the next generation of semiconductor devices," *Nature Electron.*, vol. 1, pp. 521–534, 2018.
22. K. Takeuchi *et al.*, "Random dopant fluctuation and its impact on device scaling," *IEDM Tech. Dig.*, pp. 829–832, 2001.
23. S. Datta, "Nanoscale device modelling: The Landauer approach," *Superlattices Microstruct.*, vol. 28, pp. 253–278, 2000.
24. Y. Taur *et al.*, "A continuous, analytic drain-current model for DG MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 107–109, 2004.
25. "Device performance and strain effect of sub-5 nm monolayer InP transistors," preprint, 2022.
26. "Ultrascaled double-gate monolayer SnS_2 MOSFETs for high-performance and low-power applications," *Appl. Phys. Lett.*, vol. 117, 2020.
27. Z. Khodayari *et al.*, "Computational design of sub-5 nm high-performance CMOS devices," *Appl. Surf. Sci.*, 2025.
28. H.-J. Shin *et al.*, "Promises and prospects of two-dimensional transistors," *Nature Rev. Mater.*, vol. 6, pp. 353–370, 2021.
29. D. S. Holmes *et al.*, "IRDS technology roadmaps for cryogenic electronics and quantum information processing," IEEE IRDS white paper, 2022.